REMARKS

Reconsideration of the application is requested.

Claims 1, 3, 4, 6, 7, 9, 10, and 12 are now in the application. Claims 1, 3, 4, 6, 7, 9, 10, and 12 are subject to examination. Claims 1, 3, 4, 6, 7, and 10 have been amended. Claims 2, 5, 8, and 11 have been canceled to facilitate prosecution of the instant application.

Under the heading "Claim Rejections – 35 USC § 103" on page 2 of the above-identified Office Action, claims 1, 4, 7, and 10 have been rejected as being obvious over MAFT (The MAFT Architecture for Distributed Fault Tolerance) in view of Official Notice and further in view of U.S. Patent No. 6,131,112 to Lewis et al. under 35 U.S.C. § 103.

The limitations of claim 2 have been paced into claim 1. The limitations of claim 5 have been paced into claim 4. The limitations of claim 8 have been paced into claim 7. The limitations of claim 11 have been paced into claim 10.

The dependency of claims 3 and 6 has been changed.

Claims 1, 4, 7, and 10 are not obvious for the reasons specified below.

Under the heading "Claim Rejections – 35 USC § 103" on page 10 of the above-identified Office Action, claims 2, 5, 8, and 11 have been rejected as

being obvious over MAFT (The MAFT Architecture for Distributed Fault Tolerance) in view of Official Notice, further in view of U.S. Patent No. 6,131,112 to Lewis et al. and still further in view of Published U.S. Patent Application 2002/0080930 under 35 U.S.C. § 103. Applicants respectfully traverse.

Even if the teachings in the references were combined for some reason, the claimed invention would not have been obtained.

The article entitled "The MAFT Architecture for Distributed Fault Tolerance" teaches a system in which a dedicated serial bus is used to exchange error messages in a multiprocessor system. The system described in this article is a real time control system, in particular for life-critical applications. The whole system is designed to react immediately if an error occurs. Accordingly, error messages are processed immediately.

Lewis et al. teach that messages and in particular error messages can be stored. The teaching of Lewis et al. is in the field of network management of computer systems. Administration commands and error messages are exchanged between a network management platform and computers that will be controlled. Since a person operates the network management platform, storage of the error messages is a necessity. Storage takes place in a central storage unit within the network management platform.

Cho teaches a telephone system in which state data of hardware devices (HDD, fan etc.) is first converted from parallel data to serial data by the first and second parallel-to-serial conveners (120, 140). After being transmitted, the serial data is converted back to parallel data by the serial-to-parallel converter (130) and is then stored in a central storage unit (150).

If one of ordinary skill in the art were to consider the teachings in MAFT, Lewis et al. and Cho, the only possible result would have been a system with a **centralized storage means for error messages**.

The resulting system is very different from the claimed invention in which the error messages are transmitted via the signal line and are then stored in an individual memory on each processor board.

Claims 1 and 7 specify that each processor board contains, inter alia:

> storage means;
>
> further control means responsive to the error notification signal for generating in sequence a plurality of further control signals;
>
> means responsive to one of the further control signals for converting to parallel form and storing in said storage means as error information the plurality of error signals communicated from each of the processor boards serially over said signal line; and

means connected to said storage means for reading out the error information.

Thus, error messages are transmitted via the signal line and then stored in an individual memory on each processor board. As already pointed out, the prior art suggests storing error messages at a central storage location.

Additionally, the system of claims 1 and 7 utilize an error message broadcast to realize redundant error message storage (i.e. multiple copies in different locations). No hint towards a system with a high level of redundancy of the error message storage can be found in the prior art documents. The resulting high level of redundancy of the error message storage is new and unobvious in view of the cited prior art.

Similarly claim 4 specifies that each processor board performs a step of: collecting and storing the plurality of error signals.

Claim 10 specifies: each of said processor boards communicating an error status between said processor boards by being programmed to: collect and store the plurality of error signals.

Claims 4 and 10 are also not obvious since each board collects and stores the error signals. Additionally each claim incorporates a high level of redundancy

of the error message storage and this redundancy cannot be found in the prior art documents.

Under the heading "Claim Rejections – 35 USC § 103" on page 11 of the above-identified Office Action, claims 3, 6, 9, and 12 have been rejected as being obvious over MAFT (The MAFT Architecture for Distributed Fault Tolerance) in view of Official Notice, further in view of U.S. Patent No. 6,131,112 to Lewis et al., still further in view of Published U.S. Patent Application 2002/0080930, and even further in view of U.S. Patent No. 5,410,542 to Gerbehy et al. under 35 U.S.C. § 103.

The invention as defined by claims 3, 6, 9, and 12 would not have been obtained for the reasons specified above with regard to claims 1, 4, 7, and 10.

It is accordingly believed to be clear that none of the references, whether taken alone or in any combination, either show or suggest the features of claims 1, 4, 7, or 10. Claims 1, 4, 7, and 10, are therefore, believed to be patentable over the art. The dependent claims are believed to be patentable as well because they all are ultimately dependent on one of those independent claims.

In view of the foregoing, reconsideration and allowance of claims 1, 3, 4, 6, 7, 9, 10, and 12 are solicited.

In the event the Examiner should still find any of the claims to be unpatentable, counsel would appreciate receiving a telephone call so that, if possible, patentable language can be worked out.

Please charge any fees that might be due with respect to Sections 1.16 and 1.17 to the Deposit Account of Lerner Greenberg Stemer LLP, No. 12-1099.

Respectfully submitted,

/Werner H. Stemer/
Werner H. Stemer
(Reg. No. 34,956)

MPW:cgm

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Lerner Greenberg Stemer LLP
P.O. Box 2480
Hollywood, Florida 33022-2480
Tel.: (954) 925-1100
Fax: (954) 925-1101